

CD4518B, CD4520B Types

CMOS Dual Up-Counters

High-Voltage Types (20-Volt Rating)

CD4518B Dual BCD Up-Counter
CD4520B Dual Binary Up-Counter

■ CD4518 Dual BCD Up-Counter and CD4520 Dual Binary Up-Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

The CD4518B and CD4520B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|---|--|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) | |
| Voltages referenced to V _{SS} Terminal | -0.5V to +20V |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to V _{DD} +0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | ±10mA |
| POWER DISSIPATION PER PACKAGE (P _D): | |
| For T _A = -55°C to +100°C | 500mW |
| For T _A = +100°C to +125°C | Derate Linearity at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T _A) | -55°C to +125°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | -65°C to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max | +265°C |

Features:

- Medium-speed operation – 6-MHz typical clock frequency at 10 V_{DD}
- Positive- or negative-edge triggering
- Synchronous internal carry propagation
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V
2 V at V_{DD} = 10 V
2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



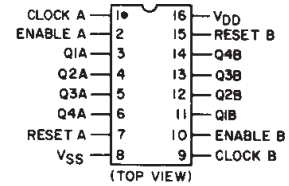
Applications:

- Multistage synchronous counting
- Multistage ripple counting
- Frequency dividers

TRUTH TABLE

| CLOCK | ENABLE | RESET | ACTION |
|-------|--------|-------|-------------------|
| | 1 | 0 | Increment Counter |
| 0 | | 0 | Increment Counter |
| | X | 0 | No Change |
| X | | 0 | No Change |
| 1 | | 0 | No Change |
| X | X | 1 | Q1 thru Q4 = 0 |

X = Don't Care 1 ≡ High State 0 ≡ Low State



**CD4518B, CD4520B
TERMINAL ASSIGNMENT**

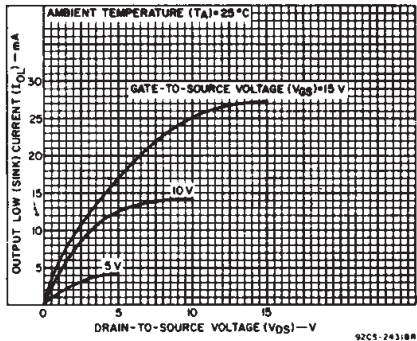


Fig. 1 – Typical output low (sink) current characteristics.

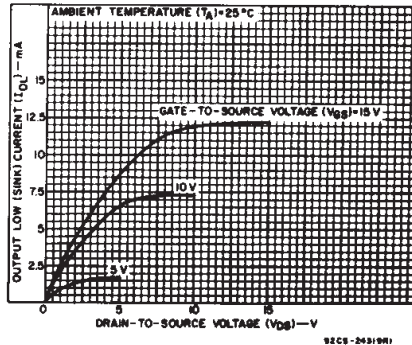


Fig. 2 – Minimum output low (sink) current characteristics.

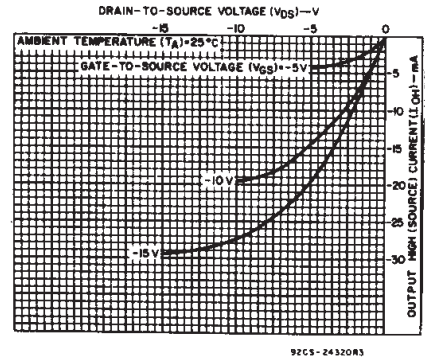


Fig. 3 – Typical output high (source) current characteristics.

CD4518B, CD4520B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|--|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | +25 | | | | | | | |
| | | | | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | — | 0,5 | 5 | 5 | 5 | 150 | 150 | — | 0,04 | 5 | μA |
| | — | 0,10 | 10 | 10 | 10 | 300 | 300 | — | 0,04 | 10 | |
| | — | 0,15 | 15 | 20 | 20 | 600 | 600 | — | 0,04 | 20 | |
| | — | 0,20 | 20 | 100 | 100 | 3000 | 3000 | — | 0,08 | 100 | |
| Output Low (Sink) Current I _{OL} Min. | 0,4 | 0,5 | 5 | 0,64 | 0,61 | 0,42 | 0,36 | 0,51 | 1 | — | mA |
| | 0,5 | 0,10 | 10 | 1,6 | 1,5 | 1,1 | 0,9 | 1,3 | 2,6 | — | |
| | 1,5 | 0,15 | 15 | 4,2 | 4 | 2,8 | 2,4 | 3,4 | 6,8 | — | |
| Output High (Source) Current, I _{OH} Min. | 4,6 | 0,5 | 5 | -0,64 | -0,61 | -0,42 | -0,36 | -0,51 | -1 | — | mA |
| | 2,5 | 0,5 | 5 | -2 | -1,8 | -1,3 | -1,15 | -1,6 | -3,2 | — | |
| | 9,5 | 0,10 | 10 | -1,6 | -1,5 | -1,1 | -0,9 | -1,3 | -2,6 | — | |
| | 13,5 | 0,15 | 15 | -4,2 | -4 | -2,8 | -2,4 | -3,4 | -6,8 | — | |
| Output Voltage: Low-Level, V _{OL} Max. | — | 0,5 | 5 | 0,05 | | | — | 0 | 0,05 | V | |
| | — | 0,10 | 10 | 0,05 | | | — | 0 | 0,05 | | |
| | — | 0,15 | 15 | 0,05 | | | — | 0 | 0,05 | | |
| Output Voltage: High-Level, V _{OH} Min. | — | 0,5 | 5 | 4,95 | | | 4,95 | 5 | — | V | |
| | — | 0,10 | 10 | 9,95 | | | 9,95 | 10 | — | | |
| | — | 0,15 | 15 | 14,95 | | | 14,95 | 15 | — | | |
| Input Low Voltage, V _{IL} Max. | 0,5, 4,5 | — | 5 | 1,5 | | | — | — | 1,5 | V | |
| | 1,9 | — | 10 | 3 | | | — | — | 3 | | |
| | 1,5, 13,5 | — | 15 | 4 | | | — | — | 4 | | |
| Input High Voltage, V _{IH} Min. | 0,5, 4,5 | — | 5 | 3,5 | | | 3,5 | — | — | V | |
| | 1,9 | — | 10 | 7 | | | 7 | — | — | | |
| | 1,5, 13,5 | — | 15 | 11 | | | 11 | — | — | | |
| Input Current I _{IN} Max. | — | 0,18 | 18 | ±0,1 | ±0,1 | ±1 | ±1 | — | ±10 ⁻⁵ | ±0,1 | μA |



Fig. 4 — Minimum output high (source) current characteristics.

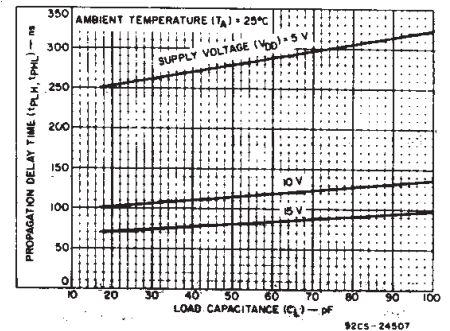


Fig. 5 — Typical propagation delay vs. load capacitance, clock or enable to output.



Fig. 6 — Typical propagation delay time vs. load capacitance, reset to output.

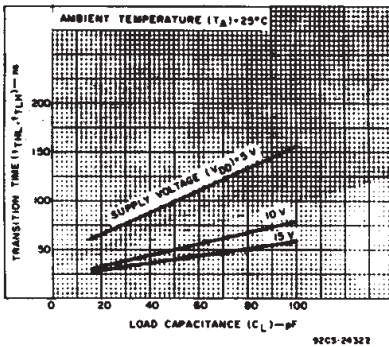


Fig. 7 — Typical transition time vs. load capacitance.



Fig. 8 — Typical maximum-clock-frequency vs. supply voltage.

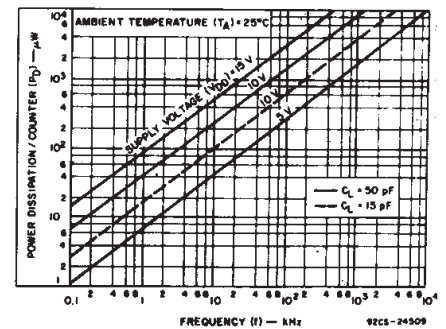


Fig. 9 — Typical power dissipation characteristics.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4518B, CD4520B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | V _{DD} (V) | LIMITS | | UNITS |
|--|------------------------|--------|------|---------------|
| | | Min. | Max. | |
| Supply Voltage Range (For T_A =Full Package Temperature Range) | | 3 | 18 | V |
| Enable Pulse Width, t_W | 5 | 400 | — | ns |
| | 10 | 200 | — | |
| | 15 | 140 | — | |
| Clock Pulse Width, t_W | 5 | 200 | — | ns |
| | 10 | 100 | — | |
| | 15 | 70 | — | |
| Clock Input Frequency, f_{CL} | 5 | | 1.5 | MHz |
| | 10 | dc | 3 | |
| | 15 | | 4 | |
| Clock Rise or Fall Time, t_{rCL} or t_{fCL} : | 5 | — | 15 | μs |
| | 10 | — | 5 | |
| | 15 | — | 5 | |
| Reset Pulse Width, t_W | 5 | 250 | — | ns |
| | 10 | 110 | — | |
| | 15 | 80 | — | |

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

| CHARACTERISTIC | TEST CONDITIONS | LIMITS | | | UNITS | |
|--|-----------------|----------------------|------|------|-------|---------------|
| | | V _{DD} V | Min. | Typ. | | Max. |
| Propagation Delay Time, t_{PHL} , t_{PLH} : Clock or Enable to Output | | 5 | — | 280 | 560 | ns |
| | | 10 | — | 115 | 230 | |
| | | 15 | — | 80 | 160 | |
| Reset to Output | | 5 | — | 330 | 650 | ns |
| | | 10 | — | 130 | 225 | |
| | | 15 | — | 90 | 170 | |
| Transition Time, t_{THL} , t_{TLH} | | 5 | — | 100 | 200 | ns |
| | | 10 | — | 50 | 100 | |
| | | 15 | — | 40 | 80 | |
| Maximum Clock Input Frequency, f_{CL} | | 5 | 1.5 | 3 | — | MHz |
| | | 10 | 3 | 6 | — | |
| | | 15 | 4 | 8 | — | |
| Minimum Clock Pulse Width, t_W | | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 35 | 70 | |
| Clock Rise or Fall Time, t_r or t_f : | | 5 | — | — | 15 | μs |
| | | 10, 15 | — | — | 5 | |
| Minimum Reset Pulse Width, t_W | | 5 | — | 125 | 250 | ns |
| | | 10 | — | 55 | 110 | |
| | | 15 | — | 40 | 80 | |
| Minimum Enable Pulse Width, t_W | | 5 | — | 200 | 400 | ns |
| | | 10 | — | 100 | 200 | |
| | | 15 | — | 70 | 140 | |
| Input Capacitance, C_{iN} | Any Input | | 5 | 7.5 | pF | |

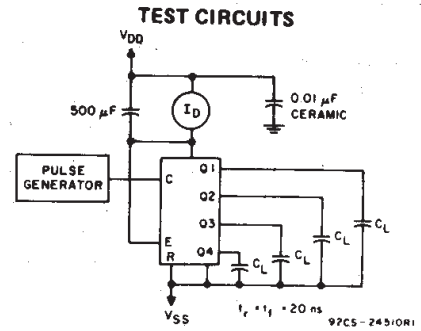


Fig. 10 — Dynamic power dissipation.

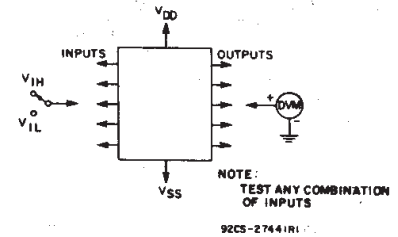


Fig. 11 — Input voltage.

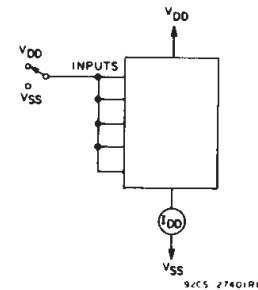


Fig. 12 — Quiescent device current test circuit.

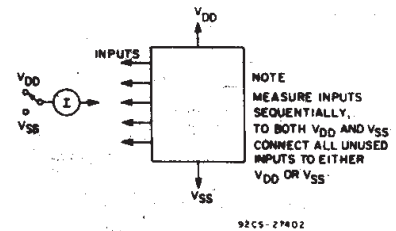


Fig. 13 — Input leakage-current test circuit.

CD4518B, CD4520B Types

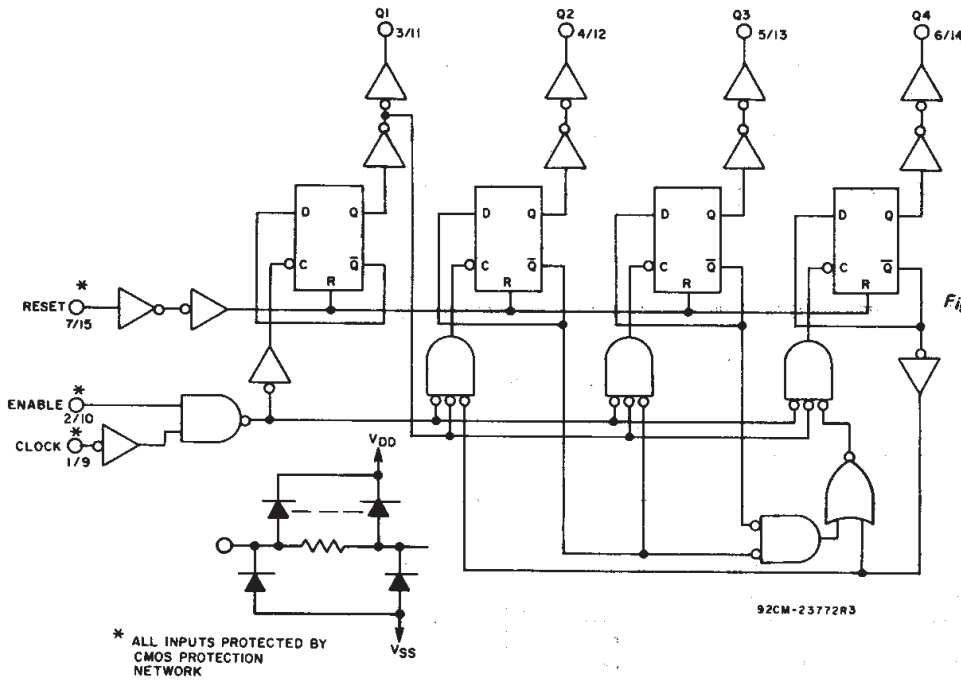


Fig. 14 — Decade counter (CD4518B) logic diagram for one of two identical counters.



Fig. 15 — Binary counter (CD4520B) logic diagram for one of two identical counters.



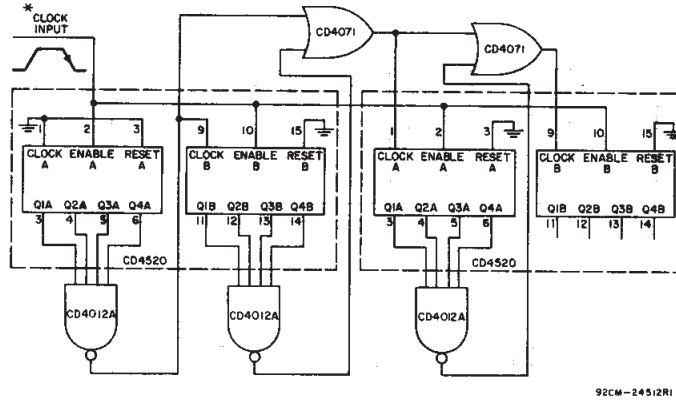
Fig. 16 — Timing diagrams for CD4518B and CD4520B.

92CM-23774R1

CD4518B, CD4520B Types



Fig. 17 — Ripple cascading of four counters with positive edge triggering.

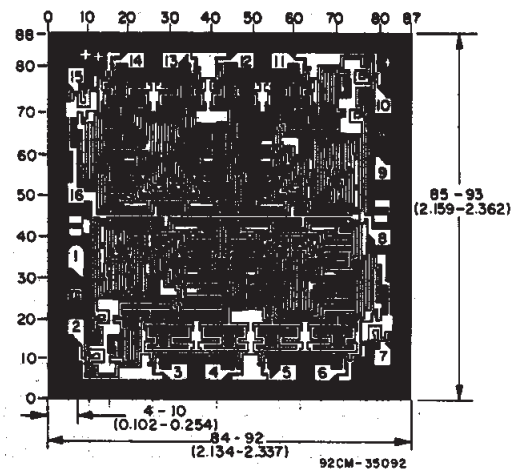


***NOTE:**
FOR SYNCHRONOUS CASCADING, THE CLOCK TRANSITION TIME SHOULD BE MADE LESS THAN OR EQUAL TO THE SUM OF THE FIXED PROPAGATION DELAY AT 15 pF AND THE TRANSITION TIME OF THE OUTPUT DRIVER STAGE FOR THE ESTIMATED CAPACITATIVE LOAD.

Fig. 18 — Synchronous cascading of four binary counters with negative edge triggering.



Dimensions and pad layout for CD4518BH chip.



Dimensions and pad layout for CD4520BH chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 7702301EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD4518BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4518BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4518BF | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD4518BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD4518BM | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BM96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BM96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BM96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BMG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BNSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4518BPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4520BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD4520BF | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD4520BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| CD4520BM | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BM96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BM96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD4520BM96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BMG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BNSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD4520BPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI

to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4518BM96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4518BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4518BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD4520BM96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4520BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4520BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4518BM96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD4518BNSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| CD4518BPWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 29.0 |
| CD4520BM96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD4520BNSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |
| CD4520BPWR | TSSOP | PW | 16 | 2000 | 346.0 | 346.0 | 29.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

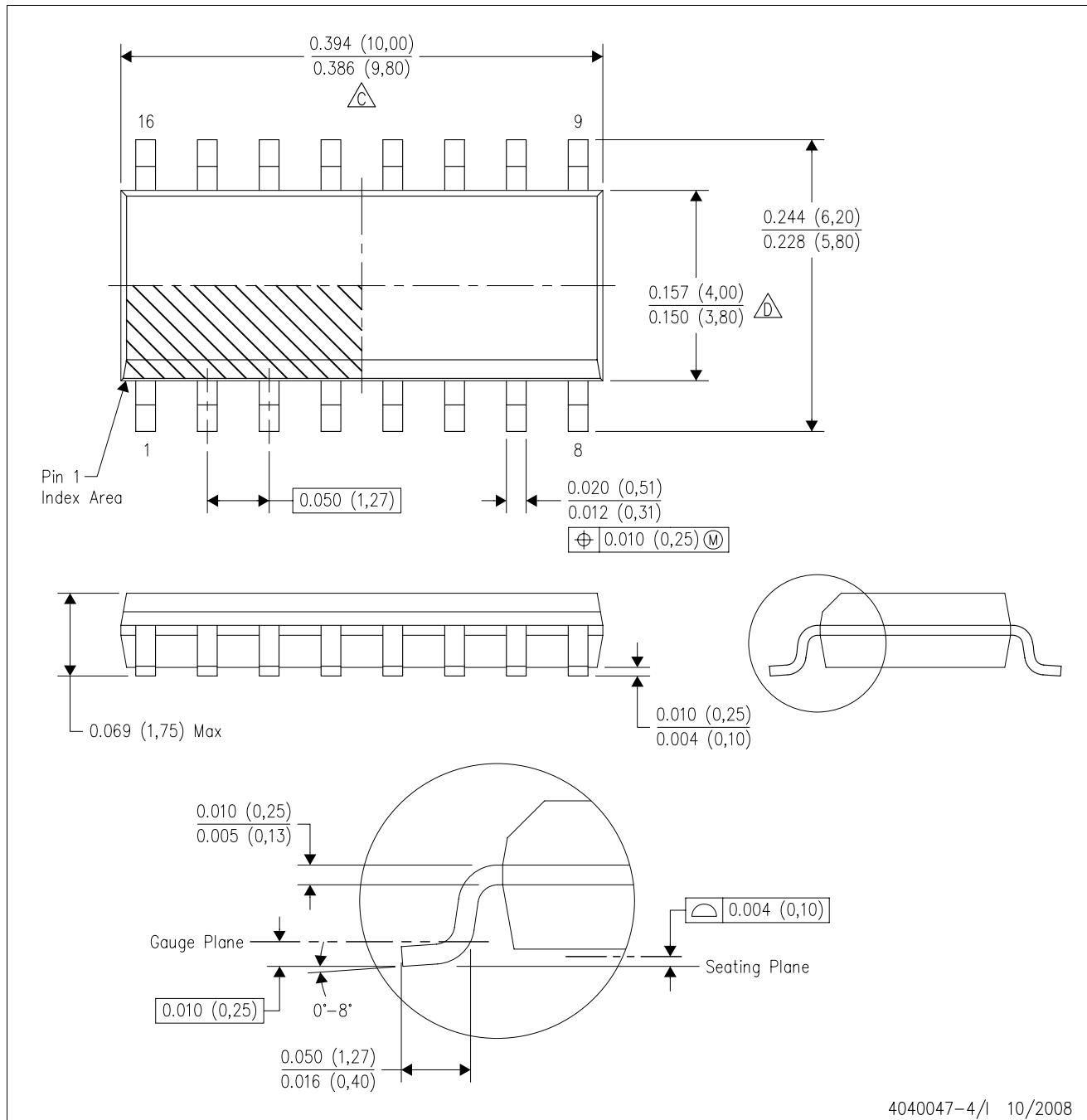


4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



4209373/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

| | |
|-----------------------------|--|
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf |

Applications

| | |
|--------------------|--|
| Audio | www.ti.com/audio |
| Automotive | www.ti.com/automotive |
| Broadband | www.ti.com/broadband |
| Digital Control | www.ti.com/digitalcontrol |
| Medical | www.ti.com/medical |
| Military | www.ti.com/military |
| Optical Networking | www.ti.com/opticalnetwork |
| Security | www.ti.com/security |
| Telephony | www.ti.com/telephony |
| Video & Imaging | www.ti.com/video |
| Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated